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10/694,822	10/29/2003	Taro Fujii	8017-1105	6783

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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	PAPER NUMBER
2183	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,822	FUJII ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,15,19 and 21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *15,19 and 21-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 9, 15, and 21-35 are pending.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15, 21, 23-25, 30, 32, 33 and 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuki in view of Stokes (U.S. Patent No. 3,537,074).

3. As per claim 15, Katsuki/Stokes discloses an array-type processor, comprising:

a multiplicity of processor elements (Fig. 1 processors 12), which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, *The examiner asserts that the processors process data and any results produced constitute event data.*

Said multiplicity of processor elements being arranged in rows and columns; *Fig. 1 shows processors 12 in rows and columns.*

A plurality of state control units that intercommunicate to realize linked operation as necessary;

An event distributing means for distributing said event data to said plurality of state control units (buses of fig. 1)

Wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data (col 12 lines 42-60 and the use of decoders suggest "code" or a preinstalled program).

Wherein each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; *The examiner asserts that each controller is connected to the one and only processor in its element area, as well as the remaining other processing elements.*

and said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units. *The examiner asserts that each controller can send data to any other controller, all of which are in other element areas. (Col. 5 lines 7-9)*

Wherein said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit (col 7 lines 52-60 – see claim 9)

Katsuki fails to disclose a single control unit and a plurality of processor elements in each element area, in which the control units are connected to the processing elements.

Stokes discloses four control units, each dedicated to a quadrant of the processing array (col 3 line 73 to col 4 line 1).

Katsuki would have been motivated to allow for a more simplistic design that saves on cost, area, and power, but still utilizes the flexibility and efficiency described in Stokes col 2 lines 30-40).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Katsuki and expand it to four separate quadrants, each controlled by a control unit, rather than have a one-to-one correspondence to the control units and processing elements. The combination allows for four separate element areas.

Regarding claim 21, Katsuki discloses an array-type processor in which a multiplicity of processor elements (col 5 lines 32-34), which individually execute data processing in accordance with instruction codes (col 12 lines 42-60) for which data is individually set (col 8 lines 26-29), are arranged in rows and columns (col 5 lines 47-53); and in which a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit (col 8 lines 26-29);

and in which state transitions of said multiplicity of processors elements are done while changing a configuration of said multiplicity of processor elements (col 8 lines 24-40), wherein: transitions of said operating states are done by a state control unit in accordance with a computer program that has been installed in advance and event data which are supplied by said multiplicity of processor elements (col 12 lines 42-60, also evident by the use of decoders and col 6 lines 3-10); said state control unit is composed of a plurality of units that intercommunicate to realize linked operation as necessary (col 5 lines 52-59); the multiplicity of said processor elements is divided into a number of element areas corresponding to the number of said plurality of state control units (col 5 lines 35-37); said number of element areas being less than said multiplicity of processor elements, said element areas being separate areas of said array-type processor that each have a plurality of processor elements; each of said plurality of state control units is connected to said processor elements corresponding to each of said plurality of state control units within respective element areas (col 5 liens 53-59); and said array-type processor includes an event distributing means for distributing said event data to said plurality of state control units that intercommunicate and realize linked operation (col 6 lines 7-10).

1. Regarding claim 23, Katsuki discloses an array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication buses that connect said plurality of state control units (see claim 22).

2. Regarding claim 24, Katsuki discloses an array-type processor according to claim 21, wherein: data buses for transmitting processing data of said plurality of processor

elements are arranged in matrix form (col 5 lines 47-53); a plurality of switch elements, which switch-control a wiring configuration of said data buses in accordance with instruction codes that are individually set as data (col 8 lines 27-29), are arranged in matrix form together with said processor elements (fig. 2); said state control units successively switch said instruction codes of said plurality of processor elements and said plurality of switch elements (col 8 lines 26-29); and said event distributing means is constituted by said data buses that are switch-controlled by said switch elements (fig 2 references 48 and 50).

3. Regarding claim 25, Katsuki discloses an array-type processor according to claim 22, wherein all of said plurality of state control units are interconnected by said event distributing means (col 5 lines 53-59).

4. Regarding claim 30, Katsuki discloses an array-type processor according to claim 21, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means (col 8 lines 26-29).

5. Regarding claim 32, Katsuki discloses an array-type processor according to claim 21, wherein one item of said event data that has been selected by said input selection means is supplied as output to said event distributing means (fig. 2—note that the router selects both inputs and outputs to the buses).

6. Regarding claim 33, Katsuki discloses an array-type processor according to claim 21, wherein output selection means is provided for each of said state control units (fig. 2), said output selection means selecting one from a plurality of items of said event data that are simultaneously received as input by said event distributing means and supplying these event data as output to said event distributing means (col 8 lines 26-29).

7. Regarding claim 35, Katsuki discloses an array-type processor according to claim 21, wherein: said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area (fig. 2); each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas (fig. 2); and said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units (col 6 lines 7-9).

3. Claims 22, 26-29, 31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuki/Stokes et al. (U.S. Patent No. 5,581,767) in view of May (U.S. Patent No. 6,414,368).

4. Regarding claim 22, Katuki/May discloses an array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication lines that connect said plurality of state control units (fig 2 reference 48 and 50).

8. Regarding claim 26, Katsuki/May discloses an array-type processor according to claim 22, wherein: said plurality of state control units are arranged in rows and columns (col 5 lines 47-52); and said state control units are connected by said event distributing means to a portion of said state control units that are located in a vicinity (col 5 lines 53-59).

9. Regarding claim 27, Katsuki/May discloses an array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to state control units that are located in eight directions in the vicinity (fig 1).

Examiner asserts that a control unit is connected to all other control units.

10. Regarding claim 28, Katsuki/May discloses an array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to said state control units that are adjacent in four row and column directions (fig 1).

Examiner asserts that a control unit is connected to all other control units.

11. Regarding claim 29, Katsuki/May discloses an array-type processor according to claim 26, wherein a central control unit is provided for distributing said event data to said plurality of state control units (col 6 lines 7-9); and said central control unit is connected by said event distributing means to all of said plurality of state control units (fig. 2).

12. Regarding claim 31, Katsuki/May discloses an array-type processor according to claim 26, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means (see claim 30).

13. Regarding claim 34, Katsuki/May discloses an array-type processor according to claim 26, wherein: said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area (fig. 2); each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas (fig. 2); and said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units (col 6 lines 7-9).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuki in view of common art.

4. As per claim 9, Katsuki discloses a multiplicity of processor elements (Fig. 1 processors 12), which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, *The examiner asserts that the processors process data and any results produced constitute event data.*

Said multiplicity of processor elements being arranged in rows and columns; *Fig. 1 shows processors 12 in rows and columns.*

A plurality of state control units that intercommunicate to realize linked operation as necessary;

An event distributing means for distributing said event data to said plurality of state control units (buses of fig. 1)

a central control unit (Fig. 2 host computer 58) is provided for distributing said event data to said plurality of state control units (Col. 6 lines 7-9); and said central control unit is connected by said event distributing means to all of said plurality of state control units. *The examiner asserts that the host is connected via buses 48, 50 and 56 according to fig. 2.*

Wherein said instruction codes of said multiplicity of processor elements are successfully switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data (col 12 lines 42-60 and the use of decoders suggest "code" or a preinstalled program).

Wherein said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit (col 7 lines 52-60)

Note that the citation shows that the transferred data includes instruction (data which causes a transition of the current state) and data (which is used for reporting to other control units the current state of a particular state control unit).

Katsuki fails to disclose that the central control unit is surrounded by said plurality of state control units.

Examiner notes that fig. 2 shows a schematic of a host computer (central control unit) that is not surrounded by the plurality of state control units. However, Examiner asserts that this drawing is only a schematic intended to show the general relationship between processing elements and in no way teaches a determined positioning of said elements.

Examiner further asserts that the actual positioning of elements of a processing device are often determined by running a sophisticated computer program. There are many variables that this computer program has to consider, but perhaps the most paramount involves minimizing the area on which processing elements are distributed and minimizing the distance of wires between elements that commonly communicate. For this reason, it would have been obvious to allow the host computer's physical location to be "surrounded" by the state control units. This appears to be an obvious and intuitive technique for minimizing both the overall area and the wire distance for the communications. Katsuki would have been motivated to utilize this physical layout for that reason.

Allowable Subject Matter

6. Claim 1 is allowed.

Response to Arguments

7. Applicant's arguments filed 19 December 2007 have been fully considered but they are not persuasive. The argument with respect to claim 1, however, is persuasive.

8. Regarding claim 15, Applicant argues that modifying Katsuki to remove the one-to-one correspondence "would change the principle of operation of Katsuki." Examiner sees nothing to support this claim. The fact that Katsuki mentions a one-to-one correspondence several times within the patent disclosure does not mean that it would not be obvious to change this aspect.

9. Regarding claim 21, Examiner does not see how the newly claimed "context" changes the scope of the claim beyond the current rejection. The claim requires, "a context, made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit and in which state transitions of said multiplicity of processors elements are done while changing the configuration of said multiplicity of processor elements." This appears only to require that the router of Katsuki properly prepares the transferred data for each cycle and that the configuration (or state) of the respect processing element is concurrently altered. Katsuki satisfies these limitations.

10. Regarding claim 9, Applicant argues that the reference "Chip Layout Optimization Using Critical Path Weighting" does not disclose claim limitations that Katsuki lacks. Examiner disagrees, by following the teachings of this reference, it would be most beneficial and, therefore, obvious to place the control circuit in the middle. This would minimize the communication path lengths. If Applicant believes this reference would lead Katsuki to a different conclusion, Applicant is invited to suggest what such an alternate conclusion may be.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183